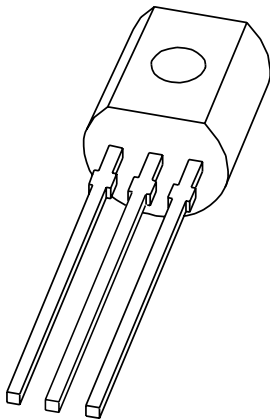


DATA SHEET



PBSS8110S

100 V, 1 A

NPN low V_{CEsat} (BISS) transistor

Product data sheet
Supersedes data of 2003 Nov 11

2004 Aug 13

100 V, 1 A
NPN low V_{CEsat} (BISS) transistor

PBSS8110S

FEATURES

- SOT54 package
- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability: I_C and I_{CM}
- Higher efficiency leading to less heat generation.

APPLICATIONS

- Automotive 42 V power
- Telecom infrastructure
- General industrial applications
- Power management
 - DC/DC converters
 - Supply line switching
 - Battery charger
 - LCD backlighting.
- Peripheral drivers
 - Generic driver (e.g. lamps and LEDs)
 - Inductive load driver (e.g. relays, buzzers and motors).

DESCRIPTION

NPN low V_{CEsat} BISS transistor in a SOT54 plastic package.

MARKING

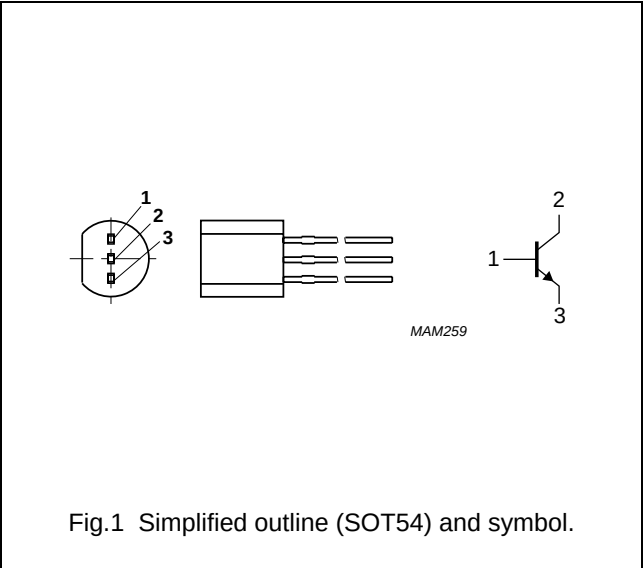
TYPE NUMBER	MARKING CODE
PBSS8110S	S8110S

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	100	V
I_C	collector current (DC)	1	A
I_{CM}	peak collector current	3	A
R_{CEsat}	equivalent on-resistance	200	m Ω

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS8110S	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	120	V
V_{CEO}	collector-emitter voltage	open base	–	100	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)		–	1	A
I_{CM}	peak collector current	$T_{j\max}$	–	3	A
I_B	base current (DC)		–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	830	mW
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C
T_{stg}	storage temperature		–65	+150	°C

Note

1. Device mounted on a FR4 printed-circuit board; single-sided copper; tinplated; standard footprint.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	150	K/W

Note

1. Device mounted on a FR4 printed-circuit board; single-sided copper; tinplated; standard footprint.

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CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$V_{CB} = 80\text{ V}; I_E = 0$	–	–	100	nA
		$V_{CB} = 80\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	–	50	μA
I_{CES}	collector cut-off current	$V_{CE} = 80\text{ V}; V_{BE} = 0$	–	–	100	nA
I_{EBO}	emitter cut-off current	$V_{EB} = 4\text{ V}; I_C = 0$	–	–	100	nA
h_{FE}	DC current gain	$V_{CE} = 10\text{ V}; I_C = 1\text{ mA}$	150	–	–	
		$V_{CE} = 10\text{ V}; I_C = 250\text{ mA}$	150	–	500	
		$V_{CE} = 10\text{ V}; I_C = 0.5\text{ A}; \text{note 1}$	100	–	–	
		$V_{CE} = 10\text{ V}; I_C = 1\text{ A}; \text{note 1}$	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 100\text{ mA}; I_B = 10\text{ mA}$	–	–	40	mV
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	–	–	120	mV
		$I_C = 1\text{ A}; I_B = 100\text{ mA}$	–	–	200	mV
R_{CEsat}	equivalent on-resistance	$I_C = 1\text{ A}; I_B = 100\text{ mA}; \text{note 1}$	–	165	200	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = 1\text{ A}; I_B = 100\text{ mA}; \text{note 1}$	–	–	1.05	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 10\text{ V}; I_C = 1\text{ A}$	–	–	0.9	V
f_T	transition frequency	$V_{CE} = 10\text{ V}; I_C = 50\text{ mA}; f = 100\text{ MHz}$	100	–	–	MHz
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = I_C = 0; f = 1\text{ MHz}$	–	–	7.5	pF

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

Technical drawing of the SOT54 package showing top, side, and lead detail views with dimension labels A, b, b₁, c, D, d, E, e, e₁, L, L₁.

0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			04-06-28 04-11-16

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PBSS8110S

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

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2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: salesaddresses@nxp.com

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Printed in The Netherlands

R75/02/pp7

Date of release: 2004 Aug 13

Document order number: 9397 750 13642

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